**Oscar Alejandro Manzano**

**EE 4513 VLSI**

**Report Lab 5**

**October 4, 2019**

For this lab, we used a new program from cadence called virtuoso, in which we are able to do the circuits inside gates. This includes the used of transistors and the materials in there. Like poly to connect then and metals. For this lab, I built a three input NAND gate and a three input NOR gate for the first part. For the second part I build four two input AND gates and two inverters, I combine then, to make the second part of it and successfully circuit as show in the picture below.

Fall 2019

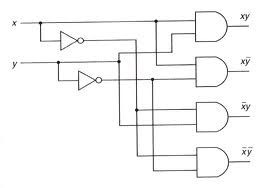
# EE 4513 – Introduction to VLSI Design

**Lab 5 - Cadence Layout Assignment**

This is a simple Cadence layout assignment. The objective of this assignment is to get familiar with the Virtuoso tool.

In this assignment, you need to do the following: -

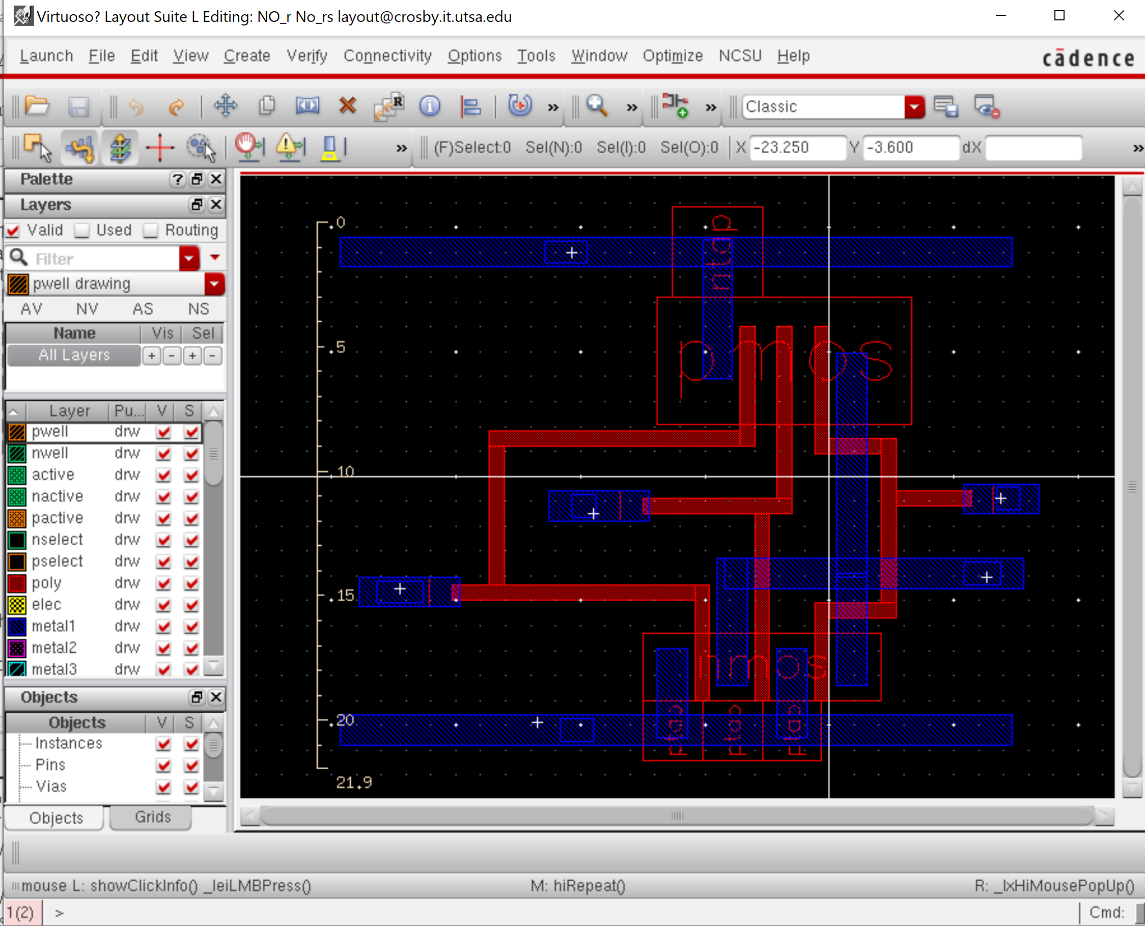
1. Create the layouts for a 3-input NAND gate and a 3-input NOR gate using Virtuoso. Verify their functionality for all input combinations using the built-in simulation tool.
2. Design and Simulate the circuit below in Virtuoso following the procedures in 1.



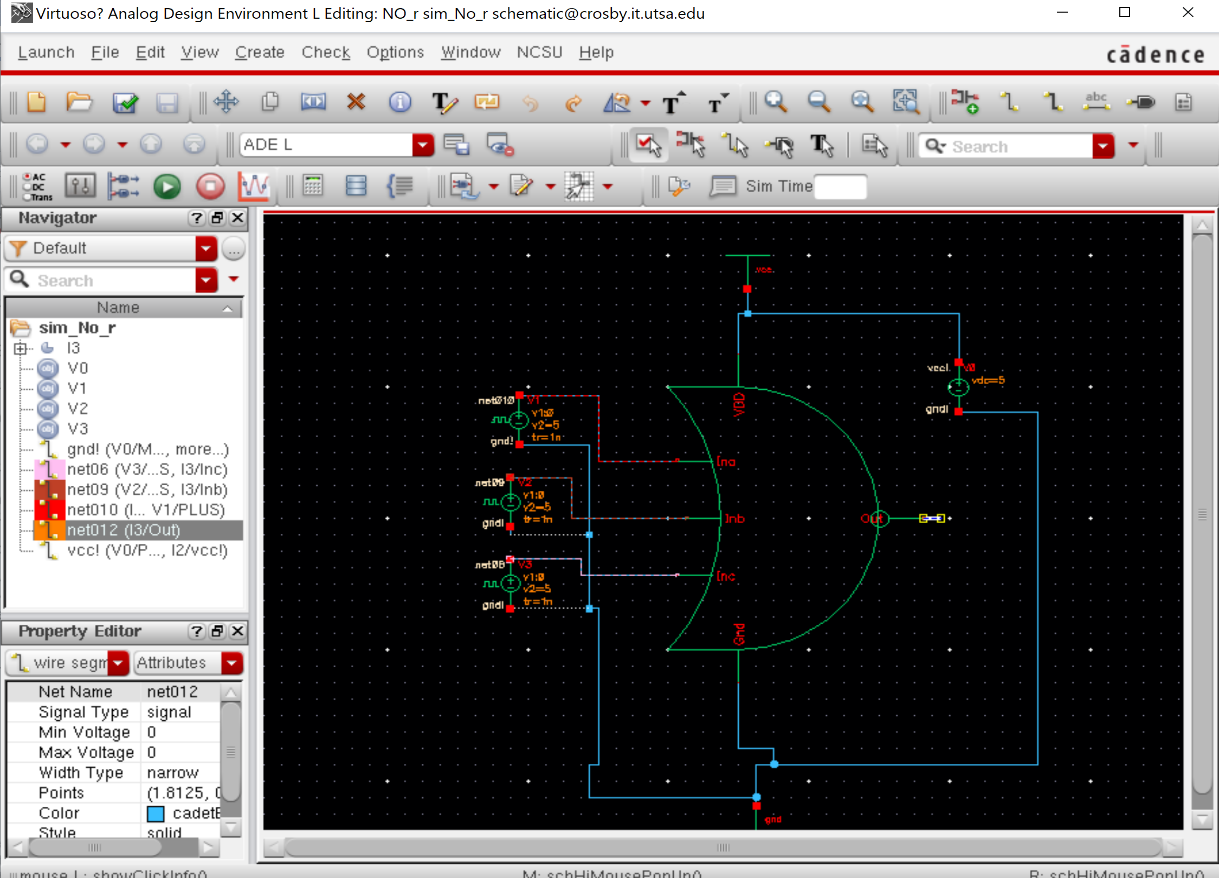
Turn in a report, which includes the following: -

1. Neat transistor level circuit schematics of the 3-input NAND gate, 3-input NOR gate and the circuit above, which you will be using to develop your layout. Also, mention the total number of transistors in each circuit.
2. The layout files for each circuit.
3. The waveforms for each circuit, showing all input combinations and their corresponding outputs.

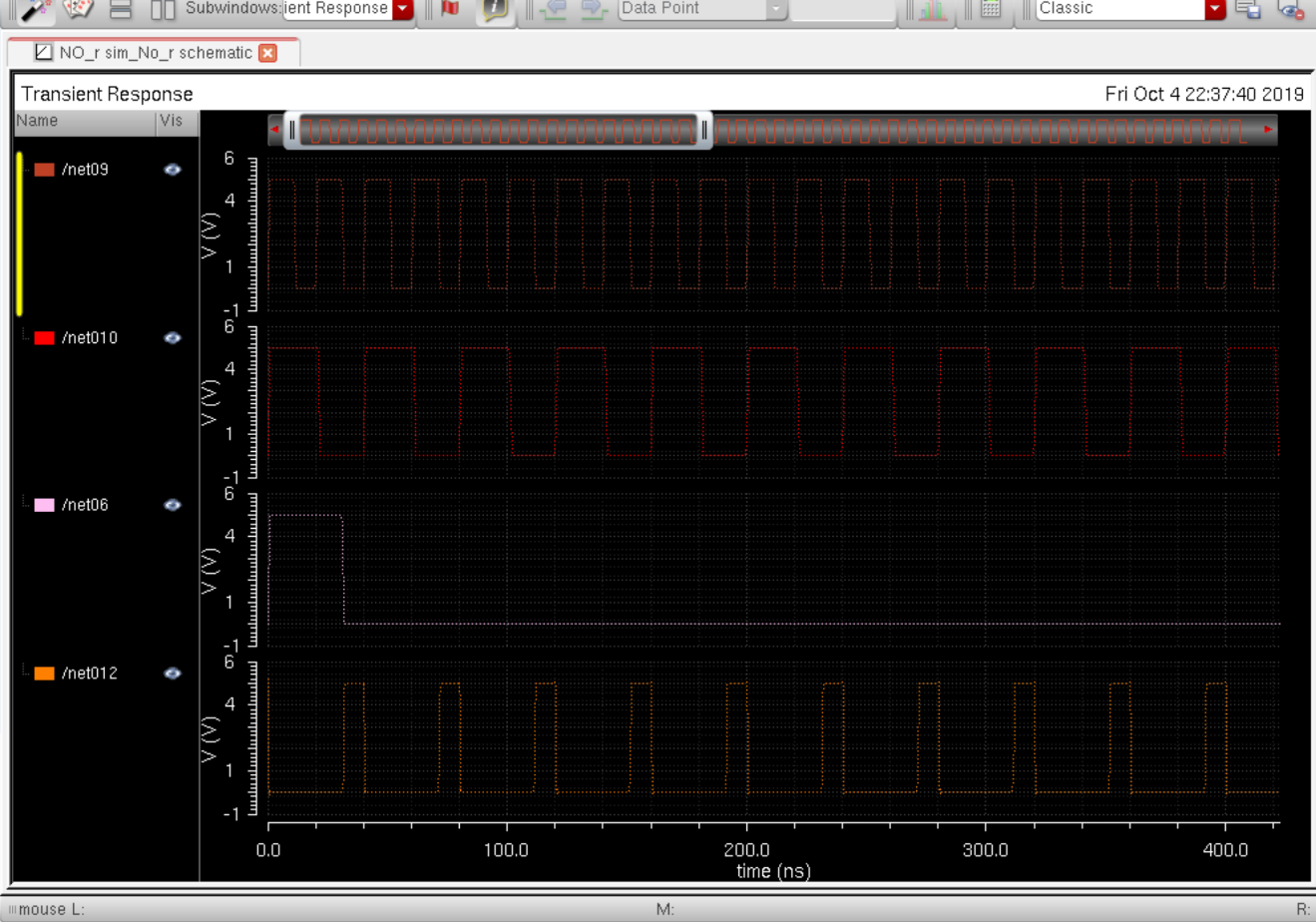
1. NOR Layout 6 transistors



Schematic

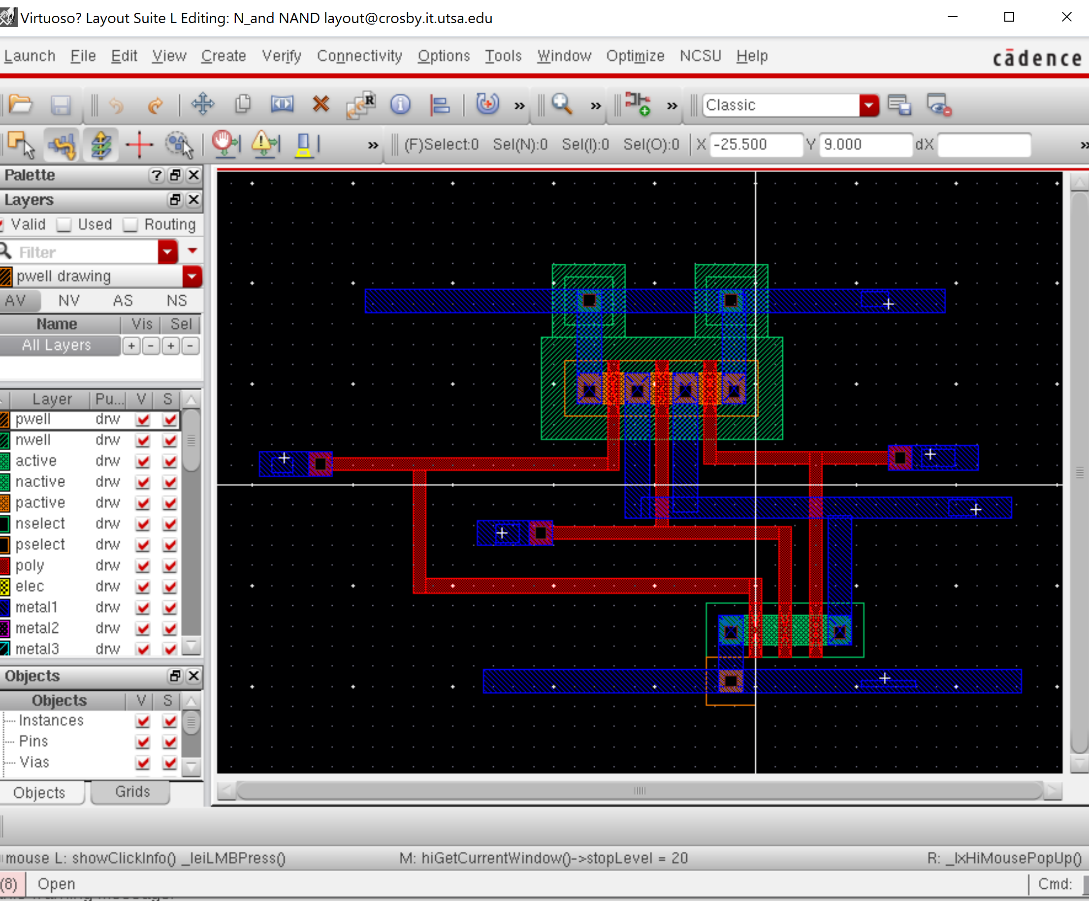


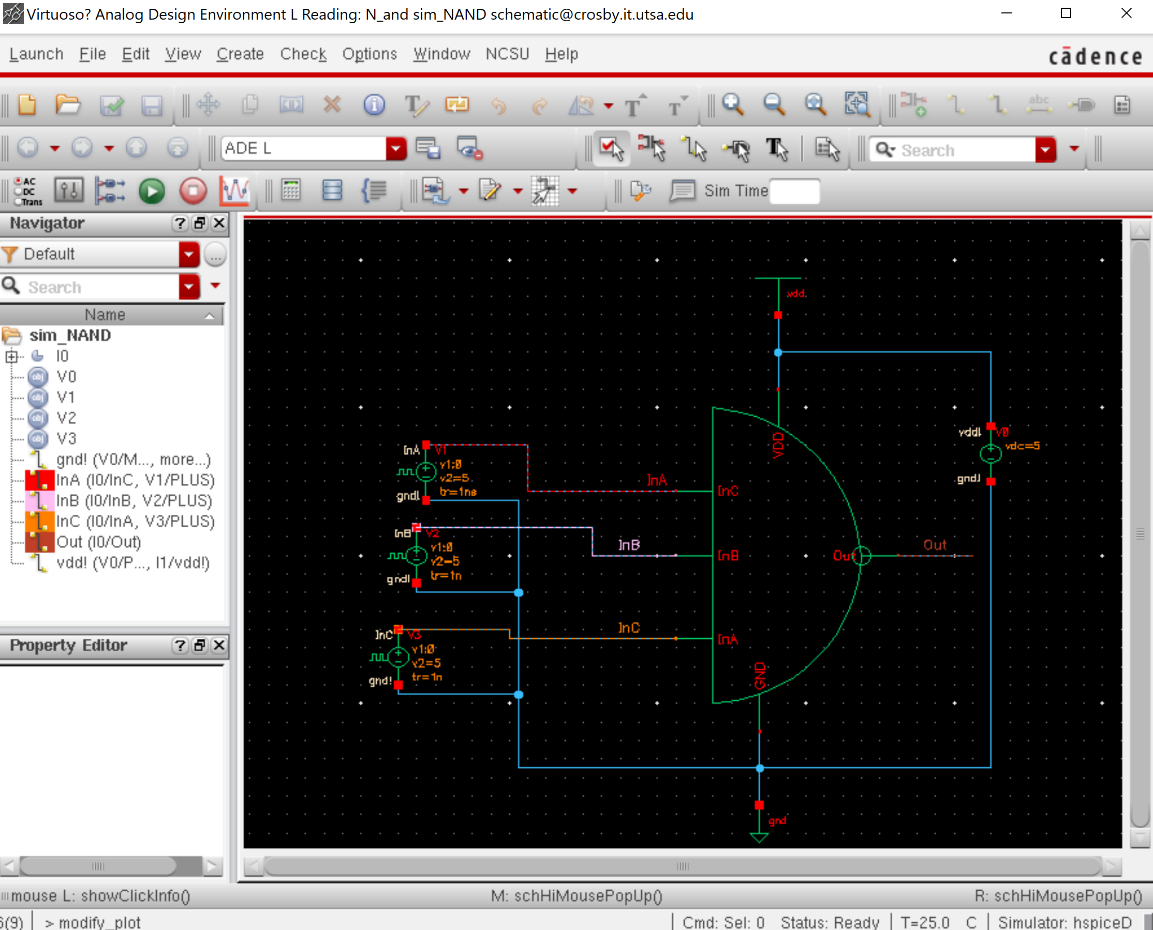
Signal



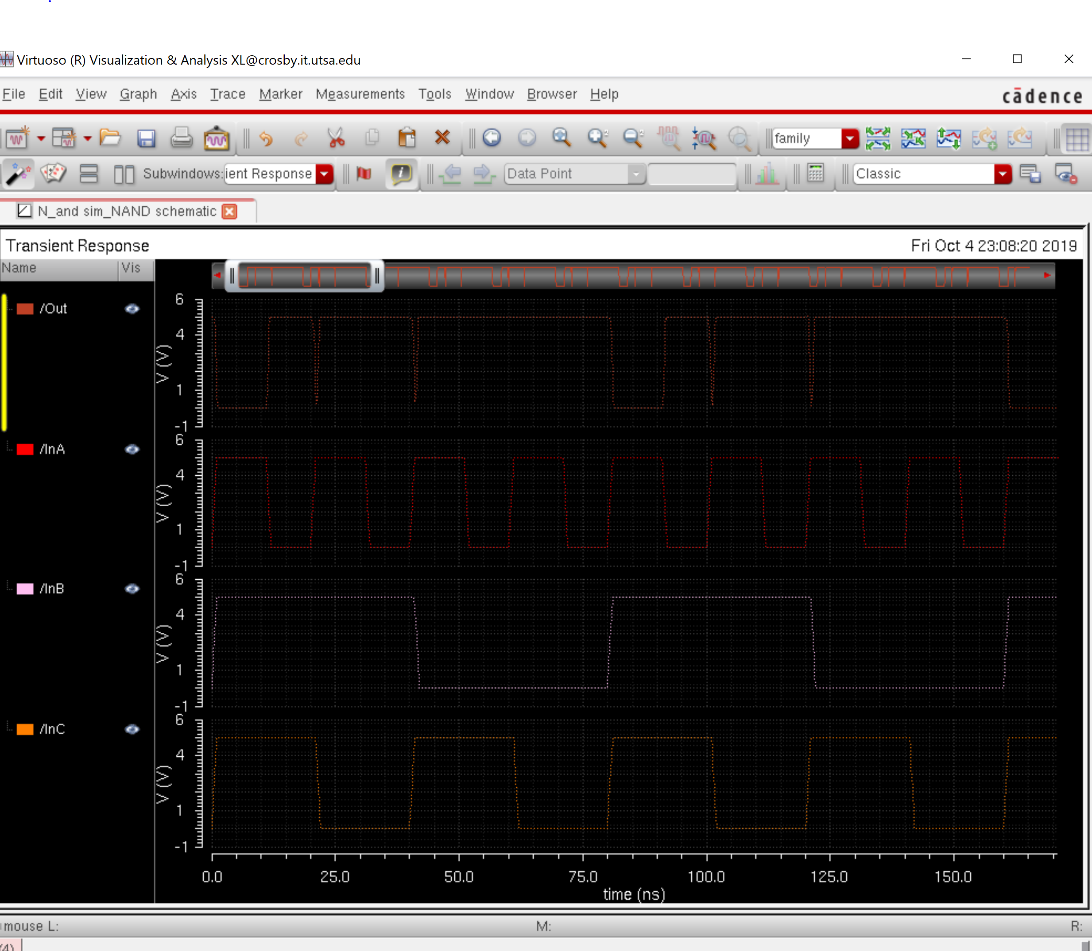
Orange=output, the other three are the inputs.

2.NAND gate 6 transistors





Signal



3.Whole circuit 28 transistors

